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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,611	09/18/2003	KokHoe Chia	STL11343	4044

7590 04/04/2006

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,611	CHIA ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-10 and 12-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,4-10 and 12-14* is/are allowed.

6)☒ Claim(s) *15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-2, 4-10, 12-17 are pending in the Application.

Claims 15-17 are rejected.

Claims 1-2, 4-10 and 12-14 are allowed.

Response to Amendment

2. Applicant's arguments and amendments filed on 23 January 2006 in response to the Office Action mailed on 21 October 2005 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuchimoto et al. (hereinafter Tsuchimoto) US Patent 6,336,202 B1.

As for claim 17, Tsuchimoto teaches a method of managing a buffer random access memory, the buffer random access memory having a first portion allocated for a defect table and a second portion allocated for data caching, the method comprising (referring to Fig. 1, the controller (element 5) is comprised of a

buffer RAM (element 14). The RAM further includes a section of memory, which is used to store a defect table (col. 3, lines 45-50 – the controller reads the defect map (table) from a disk and writes it to the RAM), and the remaining section is used for data caching (col. 3, lines 20-25 – data to be written or read is cached in the RAM)):

determining actual memory space of the first portion of the buffer random access memory occupied by the defect table to identify unused memory space of the first portion (as noted above, col. 3 lines 20-25 and 45-50 demonstrate how the RAM is divided between the defect table and data caching. The controller as illustrated in Fig. 1 must inherently make a determination which data in the RAM is the defect table and which area in the RAM is for data caching in order for Tsuchimoto's system to work); and

reallocating the unused memory space of the first portion of the buffer random access memory for use in data caching (the remaining memory area in the RAM, not being used to store the variable sized defect table can now be used (i.e. allocated) for data caching purposes. Referring to col. 5, lines 57-67, Tsuchimoto aims at minimizing the size of the defect map so that it occupies a minimal amount of the RAM in the controller. The remaining area of the RAM is now allocated for data caching purposes as described in col. 3, lines 20-25).

Additionally, it is worthy to note that Tsuchimoto teaches the use of a reassign table in col. 6, lines 43-65. This reassign table (which is also referred to as the defect map) can be produced either before *or after* (emphasis added) logical formatting. In other words, an original defect map can be produced, and then subsequently updated

to account of any change in the sectors that are identified during use of disk drive unit. Any changes that are required recorded in the reassign table, which can be written to the RAM at a later time. Please refer to col. 7, lines 6-26. In other words, the table may be originally created, and then subsequently updated to provide address information on sectors that fail or become defect after LBAs are assigned. The table is modified, hence the amount of memory required to store the information will change (recall the table is of variable length), resulting in a change in amount of memory remaining in the RAM for caching purposes. When the table is rewritten, the system will automatically reallocate memory in the RAM based on the determination of how much memory is available within the RAM.

As for claims 15-16 Tsuchimoto teaches a disk drive unit (i.e. mass storage device) comprising a controller (element 5), which controls an MPU (element 12) and an HDC (element 11), used to execute control over the data storage system (col. 3, lines 18-25).

Response to Arguments

4. Applicant's arguments and amendments filed on 23 January 2006 with respect to newly added claims 15-17 have been fully considered but they are not persuasive.

As for claim 15, Applicant contends that in light of the newly amended preamble of the claim, Tsuchimoto fails to meet the first limitation of the claim (i.e. "determining actual memory space ..."). More specifically, Applicant asserts that Tsuchimoto fails to teach identifying unused buffer RAM memory in the portion of the buffer RAM allocated

for the defect table. Applicant additionally contends that Tsuchimoto fails to teach actually reallocating unused memory space from the previous defect table allocation to a new data cache allocation as claimed in the instant application.

Examiner however maintains that Tsuchimoto teaches the use of a reassign table in col. 6, lines 43-65. This reassign table (which is also referred to as the defect map) can be produced either before *or after* (emphasis added) logical formatting. In other words, an original defect map can be produced, and then subsequently updated to account of any change in the sectors that are identified during use of disk drive unit. Any changes that are required recorded in the reassign table, which can be written to the RAM at a later time. Please refer to col. 7, lines 6-26. In other words, the table may be originally created, and then subsequently updated to provide address information on sectors that fail or become defect after LBAs are assigned. The table is modified, hence the amount of memory required to store the information will change (recall the table is of variable length), resulting in a change in amount of memory remaining in the RAM for caching purposes. When the table is rewritten, the system will automatically reallocate memory in the RAM based on the determination of how much memory is available within the RAM.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

6. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

3/30/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER